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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,533	02/27/2002	Hiroshi Hashimoto	020244	6400

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER

LE, THAO X

ART UNIT PAPER NUMBER

2814

DATE MAILED: 01/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Office Action Summary

Application No. 10/083,533	Applicant(s) HASHIMOTO ET AL.	
Examiner Thao X Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 October 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 and 40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 and 40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

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DETAILED SUPPLEMENTAL ACTION

1. The amendment filed on 10/17/03, in the Remarks section page 16 first paragraph, the Applicant indicated that claims 6 and 9-15 have been canceled. According to the Applicant's Attorney, Mr. Michael Lau, the cancellation was a typographical error; thus this supplemental Final Office Action is considering the cancelled claims 6, and 9-15.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-5, 7-12, 14-15 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (APA) in view of US 6544845 to Yoo et al.

Regarding to claims 1, APA discloses a semiconductor integrated circuit (IC) device fig. 1Q, comprising: a substrate 11, a nonvolatile memory device 16F formed in a memory cell region (flash memory cell A), of substrate 11 and having a multilayer gate electrode structure comprising a tunnel insulating film 12A covering substrate 11 and floating gate electrode 13A formed on the tunnel insulating film 12A and having a side wall surfaces covered with a protection insulating film formed of an oxide 16S; and a semiconductor device (transistor) formed in a device region of substrate 11, the semiconductor device comprising a gate insulating film 12B covering substrate 11 and gate electrode 16B formed on the gate insulating film 12B, the gate insulating film 12B is interposed between substrate 11 and the gate electrode 2B have a substantially uniform thickness, fig. 1Q, an impurity concentration of a source region of said nonvolatile memory device is increased (area 11b), specification page 6 lines 10-20, so as to reduce concentration of an electric field on an edge of the floating gate electrode, the concentration of the electric field being caused by a high voltage applied to the source region at a time of erasing an electric charge from said nonvolatile memory device.

But, APA does not discloses the device wherein a bird's beak structure is formed of oxide film at an interface of the tunnel insulating film and the floating gate electrode, the bird's beak structure penetrating into the floating gate electrode along the interface from the sidewall faces of the floating gate electrode and the bird's beak structure increases a thickness of the tunnel insulating film at the edge of the floating gate electrode so as to prevent the tunnel insulation film from being degraded by the concentration of the electric field on the edge of the floating gate electrode.

However, Yoo reference discloses a device wherein a bird's beak structure 518, fig. 11, column 4 line 25-34 and column 9 line 10, is formed of oxide film at an interface of the tunnel insulating film 502A and the floating gate electrode 504A, the bird's beak structure penetrating into the floating gate electrode 504A along the interface from the sidewall faces of the floating gate electrode 504A, and the bird's beak structure increases a thickness of the tunnel insulating film at the edge of the floating gate electrode, fig. 11, so as to prevent the tunnel insulation film from being degraded by the concentration of the electric field on the edge of the floating gate electrode. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the bird's beak structure teaching of Yoo with APA's device, because the bird's peak would have improved the performance of IC nonvolatile memory as taught by Yoo, column 4 lines 8-19.

The process limitations "the thermal" in claim 1, does not carry weight in a claim drawn to structure. *In re Thorpe*, 277 USPQ 964 (Fed. Cir. 1985).

With respect to 'so as to reduce concentration of an electric field on an edge of the floating gate electrode, the concentration of the electric field being caused by a high voltage applied to the source region at a time of erasing an electric charge from said nonvolatile memory device and so as to prevent the tunnel insulation film from being degraded by the concentration of the electric field on the edge of the floating gate electrode', such limitations is obvious because the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be obvious. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

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Regarding to claims 2-5, 10-12 APA discloses the IC device wherein the multiplayer gate electrode structure further comprises an insulating film 14A, fig. 1H, formed on the floating gate electrode 13A and a control gate electrode 16A formed on the insulated film 13A, wherein each of the gate electrode and control gate electrode comprises doped polysilicon, specification page 4 lines 20-35, wherein the oxide film forming the protection insulating film connects to the bird's beak structure, wherein the protection insulating film 18 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure, fig. 1K.

Regarding to claims 7-8, 14-15, APA discloses the IC device having the tunnel oxide 12, spec. page 2 or nitride, page 4.

Regarding claim 9, APA discloses a semiconductor integrated circuit device in fig. 7M comprising: a substrate 11, a nonvolatile memory device formed in a memory cell region of said substrate, the nonvolatile memory device comprising: a first active region 11a covered with a tunnel insulating film 12A; a second active region 11b formed next to the first active region and covered with an insulating film 12A, a control gate formed of an embedded diffusion region 11c formed in the second active region; a first gate electrode 13A extending on the tunnel insulating film 12A in the first active region 11a and forming a bridge between the first and second active regions to be capacitive-coupled via the insulating film 12A to the embedded diffusion region 11c in the second active region 11b, the first gate electrode 13A having sidewall faces thereof covered with a protection insulating film 18 formed of a thermal oxide film; and a diffusion region 11a, 11b, and 11c formed on each of sides of the first gate electrode 13A in the first active region; and a semiconductor device (transistor) formed in a device region of said substrate, the semiconductor device comprising a gate insulating film 12b covering said substrate and a second

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gate electrode 13b formed on the gate insulating film, the first gate electrode along the interface from the sidewall faces of the first gate electrode; and the gate insulating film 12B is interposed between said substrate 11 and the second gate electrode 13B to have a substantially uniform thickness.

But, APA does not disclose the device wherein a bird's beak structure is formed of oxide film at an interface of the tunnel insulating film and the floating gate electrode, the bird's beak structure penetrating into the floating gate electrode along the interface from the sidewall faces of the floating gate electrode and the bird's beak structure increases a thickness of the tunnel insulating film at the edge of the floating gate electrode so as to prevent the tunnel insulation film from being degraded by the concentration of the electric field on the edge of the floating gate electrode.

However, Yoo reference discloses a device wherein a bird's beak structure 518, fig. 11, column 4 line 25-34 and column 9 line 10, is formed of oxide film at an interface of the tunnel insulating film 502A and the floating gate electrode 504A, the bird's beak structure penetrating into the floating gate electrode 504A along the interface from the sidewall faces of the floating gate electrode 504A, and the bird's beak structure increases a thickness of the tunnel insulating film at the edge of the floating gate electrode, fig. 11, so as to prevent the tunnel insulation film from being degraded by the concentration of the electric field on the edge of the floating gate electrode. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the bird's beak structure teaching of Yoo with APA's device, because the bird's peak would have

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improved the performance of IC nonvolatile memory as taught by Yoo, column 4 lines 8-19.

Regarding claim 40, as discussed in the above claim 1-5,7-8, the APA and Yoo disclose all the limitations of claim 40.

5. Claims 6, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (APA) and US 6544845 to Yoo et al as applied to claim 1, and further in view of US 6406959 to Prall et al.

Regarding claims 6, 13, APA and Yoo do not expressly disclose the semiconductor IC device wherein a SOI substrate is employed as substrate.

However, Prall reference discloses a flash memory device wherein the substrate 11 can be either silicon or SOI, column 4 line 15. At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to replace the silicon substrate of APA with either Si or SOI substrate teaching of Prall, because such substrate substitution would have been considered a mere substitution of art-recognized equivalent values.

Response to Arguments

6. Applicant's arguments with respect to claims 1-5, and 7-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

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7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

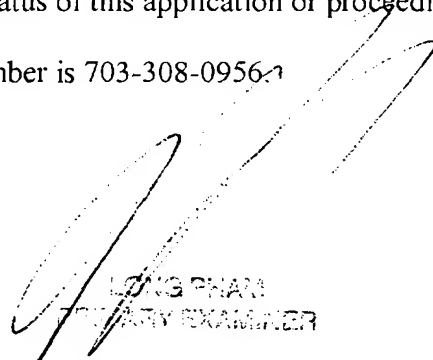
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
13 Jan 04



LONG PHAN
PATENT EXAMINER